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Development of a USN HDR LOS Modem Prototype and the Implementation of a OFDM Waveform

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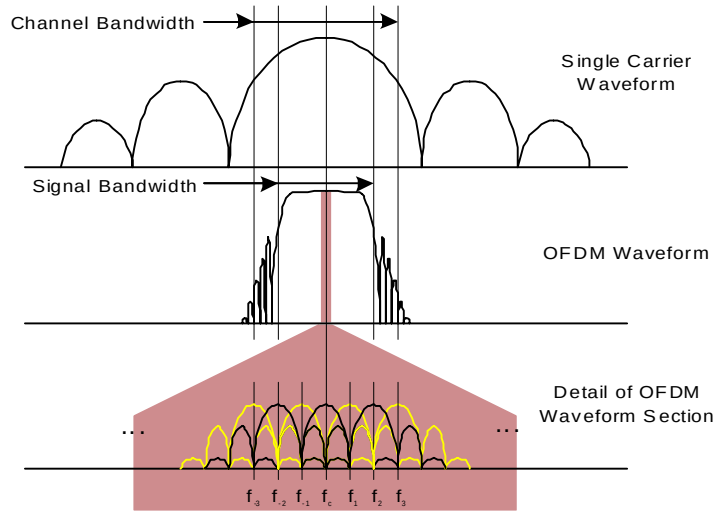
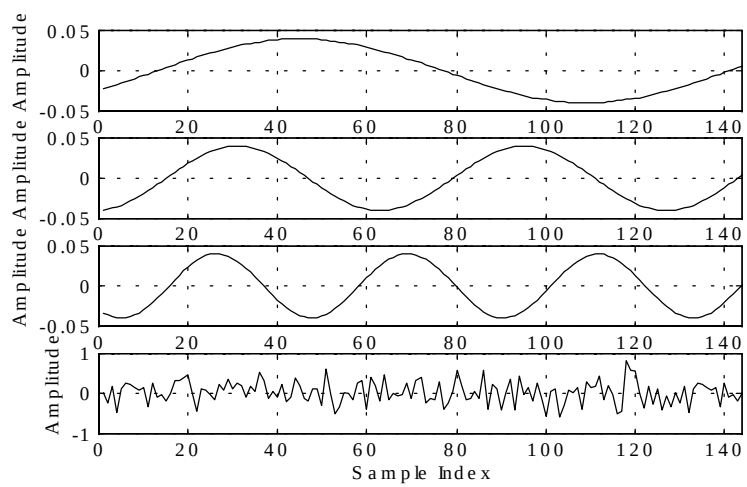
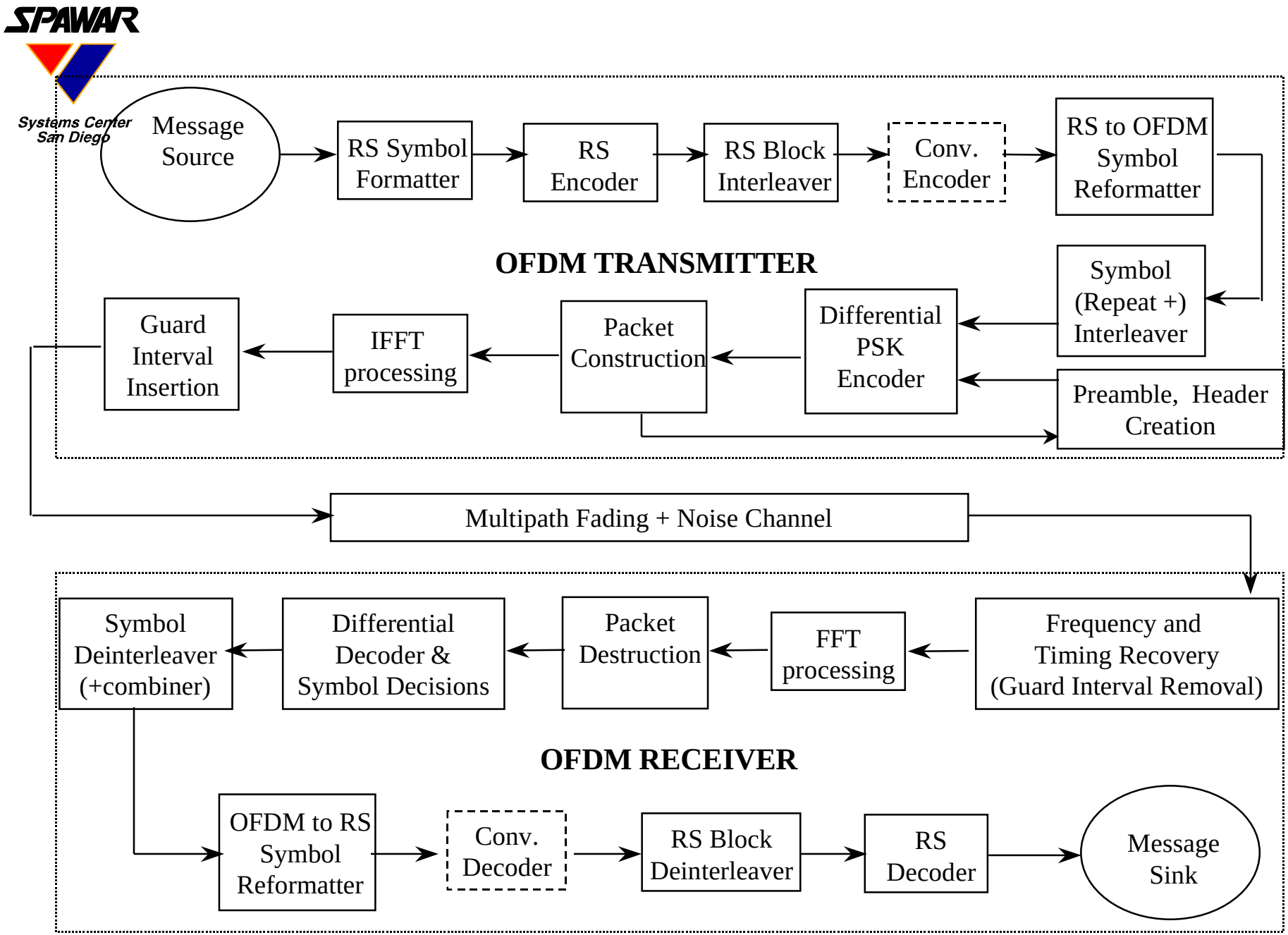
Overview of OFDM Waveform

Fundamentals of OFDM

- OFDM consists of a set of orthogonal tones where each tone is independently modulated
- Modulation/Demodulation is efficiently accomplished with the FFT
- Guard interval is added to absorb intersymbol interference (instead of adaptive equalization)
- OFDM offers:
  - Improved spectral containment.
  - Less intersymbol interference.
  - Less sensitive to impulsive interference.



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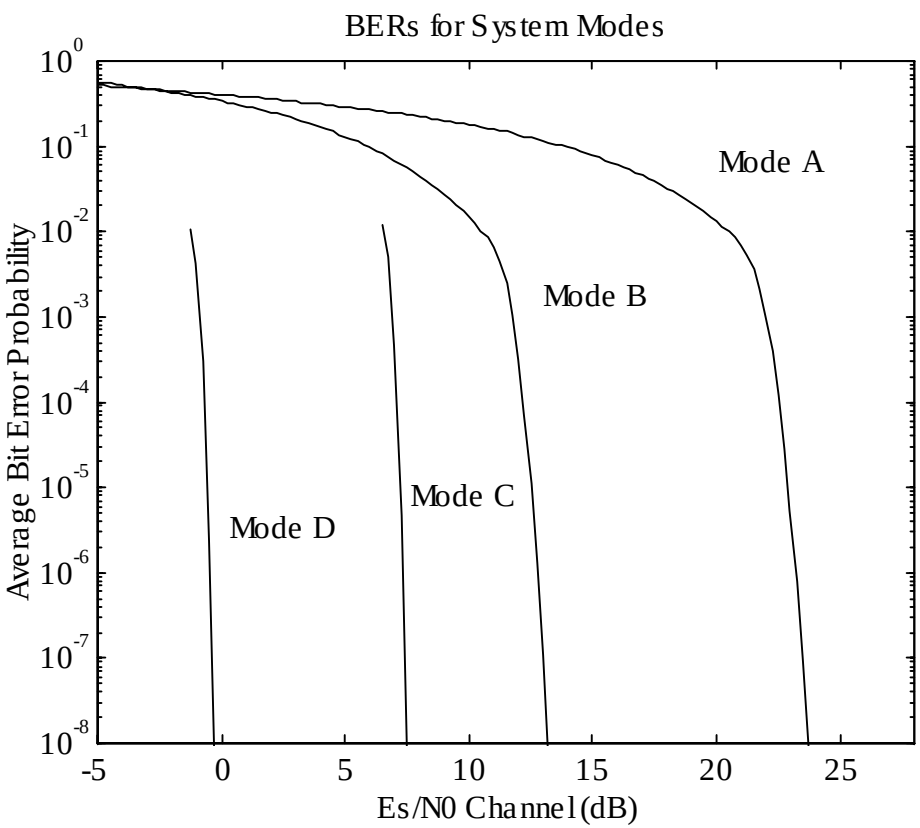
Message Source
RS Symbol Formatter
RS Encoder
RS Block Interleaver
Conv. Encoder
RS to OFDM Symbol Reformatter
OFDM TRANSMITTER
Symbol (Repeat +) Interleaver
Differential PSK Encoder
Packet Construction
IFFT processing
Guard Interval Insertion
Preamble, Header Creation
Multipath Fading + Noise Channel
Frequency and Timing Recovery (Guard Interval Removal)
FFT processing
Packet Destruction
Differential Decoder & Symbol Decisions
Symbol Deinterleaver (+combiner)
OFDM RECEIVER
OFDM to RS Symbol Reformatter
Conv. Decoder
RS Block Deinterleaver
RS Decoder
Message Sink

Modes of Operation for OFDM Waveform

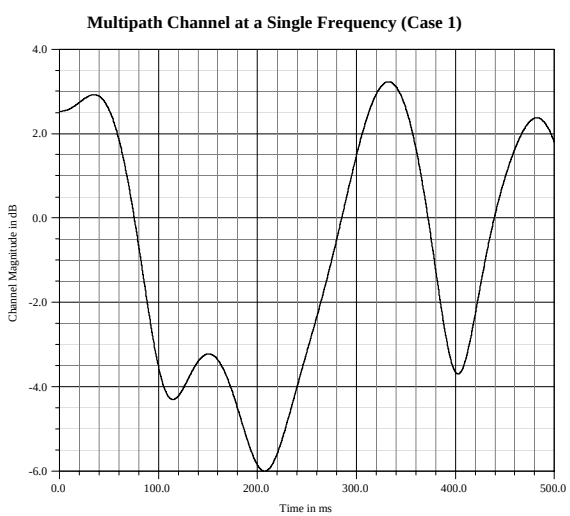
- Four operating modes specified by NPS, NOVA, and SSC-SD all within 480 kHz 3dB BW / 600 kHz channel.
- Analysis indicates AWGN performance limits at:
  - Mode A: 1536 kbps, D16PSK, RS, 24 dB SNR
  - Mode B: 768 kbps, DQPSK, RS, 13 dB SNR
  - Mode C: 384 kbps, DQPSK, conv. 1/2, RS, 7.5 dB SNR
  - Mode D: 64 kbps, DQPSK, DSSSx5, conv. 1/2, RS, -0.2 dB SNR



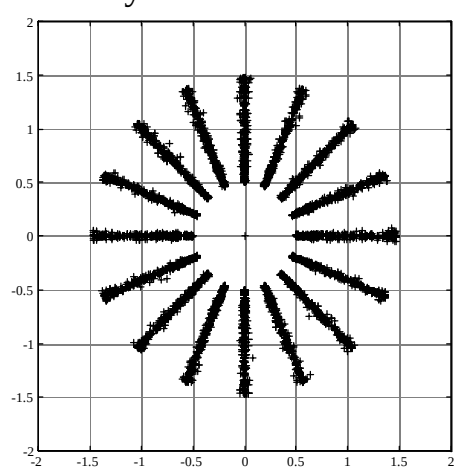
RS = Reed Solomon FEC code

OFDM Operation in UHF Channel #1
(D16-PSK, no FEC)

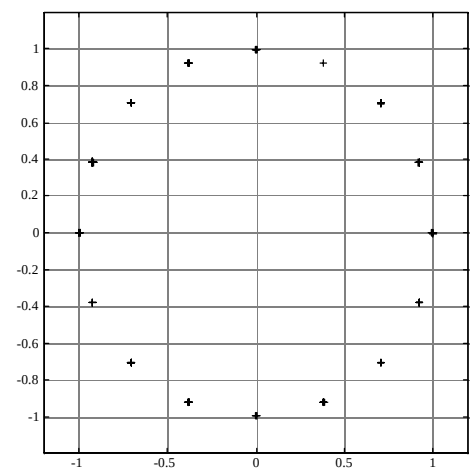
- Propagation loss = 130 dB, Cable/Misc. loss = 5 dB, Path #1 has a Rician characteristic with a Doppler spread of 1 Hz. Path #2 has a Rayleigh distribution with a mean path delay of 0.01 us, a loss (relative to Path #1) of 6 dB, and a Doppler spread of 10 Hz.
- Path characterized as flat fading.



Overlay of 200 OFDM Tones

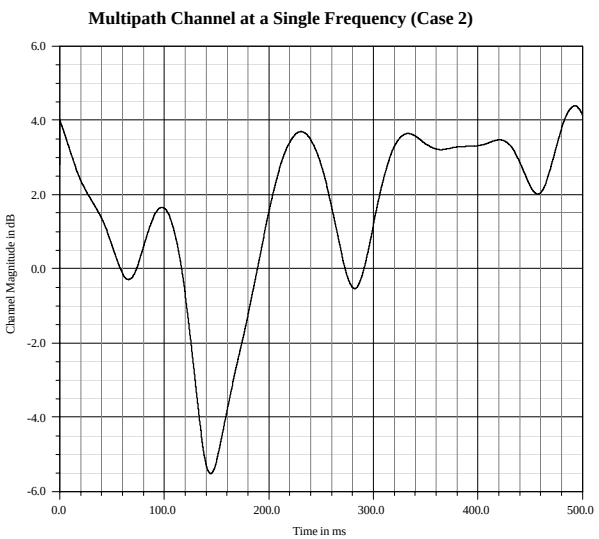


Detection of Tone 7

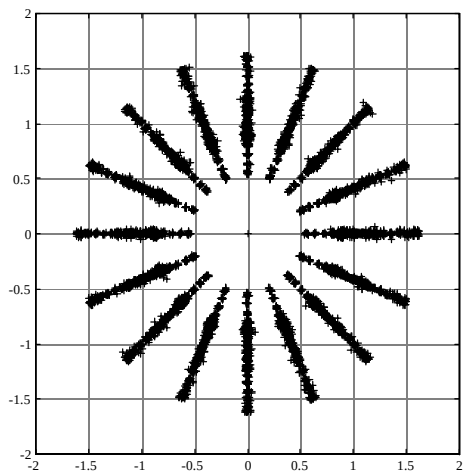


OFDM Operation in UHF Channel #2
(D16-PSK, no FEC)

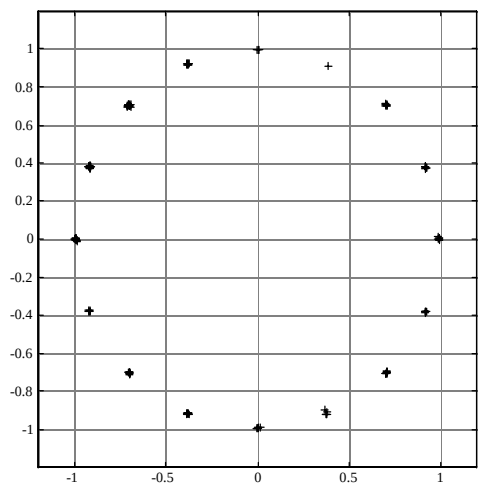
- Propagation loss = 130 dB, Cable/Misc. loss = 5 dB, Path #1 has a Rician characteristic with a Doppler spread of 10 Hz. Path #2 has a Rayleigh distribution with a mean path delay of 0.07 us, a loss (relative to Path #1) of 5 dB, and a Doppler spread of 10 Hz. Path #3 has a Rayleigh distribution with a mean path delay of 0.80 us, a loss (relative to Path #1) of 15 dB, and a Doppler spread of 10 Hz.
- Path characterized as combination flat and selective fading.



Overlay of 200 OFDM Tones

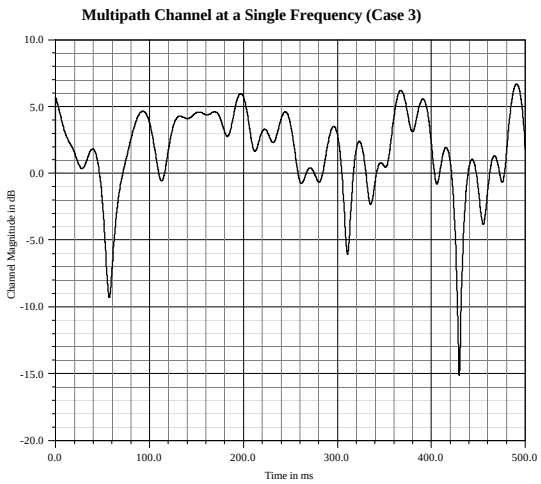


Detection of Tone 7

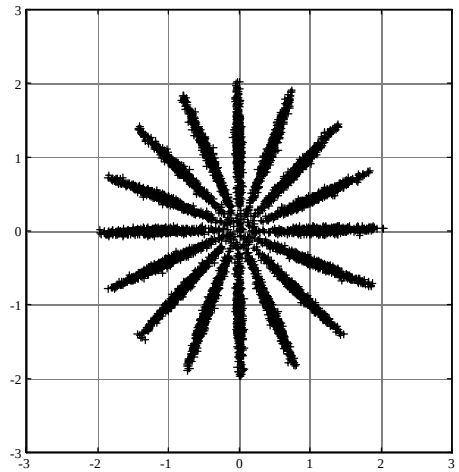


OFDM Operation in UHF Channel #3
(D16-PSK, no FEC)

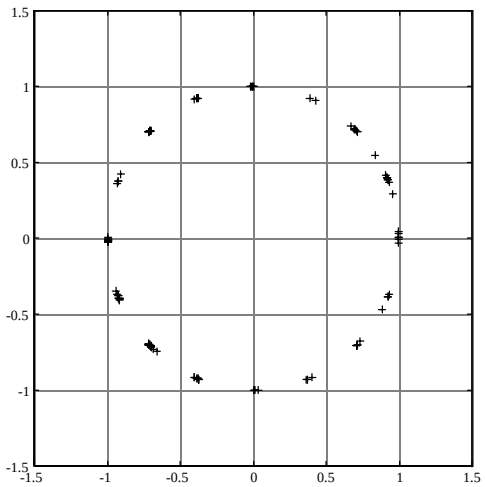
- Propagation loss = 130 dB, Cable/Misc. loss = 5 dB, Path #1 has a Rician characteristic with a Doppler spread of 25 Hz. Path #2 has a Rayleigh distribution with a mean path delay of 0.9 us, a loss (relative to Path #1) of 3 dB, and a Doppler spread of 25 Hz. Path #3 has a Rayleigh distribution with a mean path delay of 5.1 us, a loss (relative to Path #1) of 9 dB, and a Doppler spread of 25 Hz.
- Path characterized as selective fading.



Overlay of 200 OFDM Tones



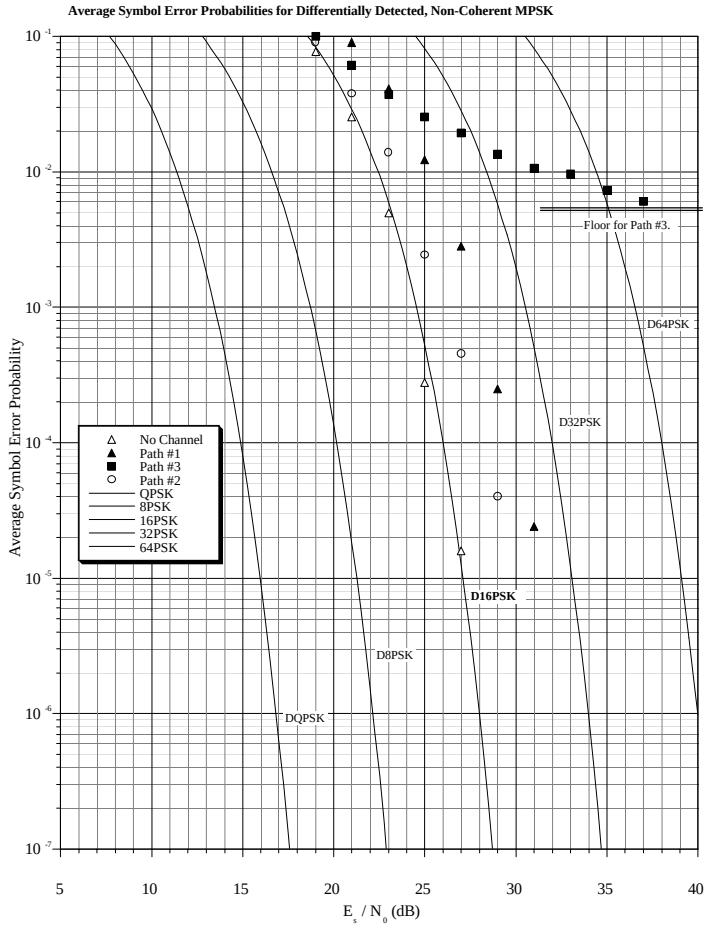
Detection of Tone 7



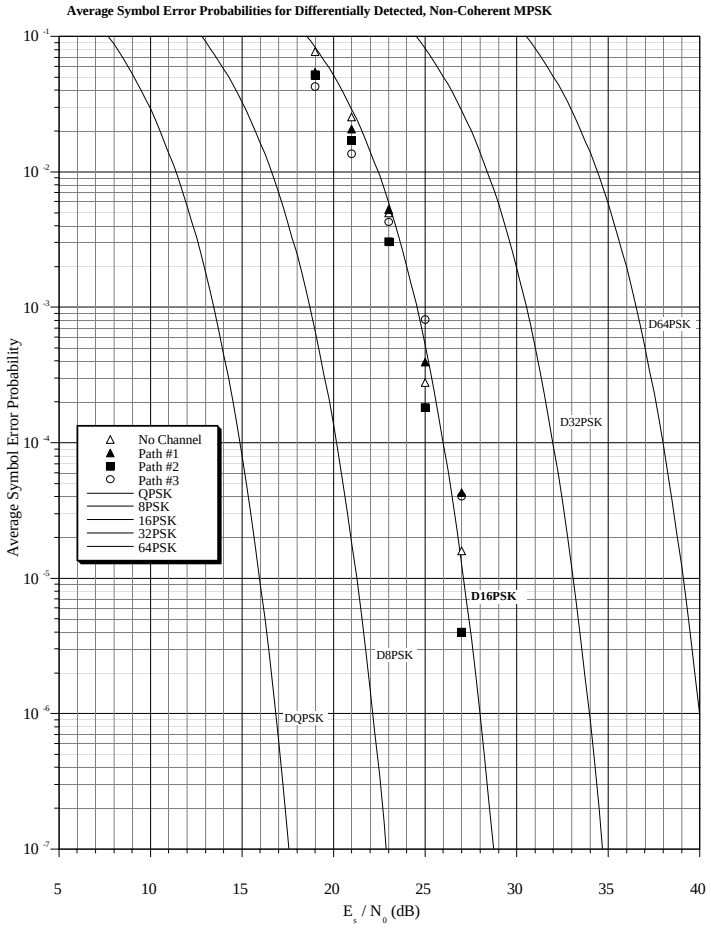
OFDM Operation in UHF Channels #1-3

(D16-PSK, no FEC)

without Spatial Diversity



with Spatial Diversity



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Modem
Hardware Development

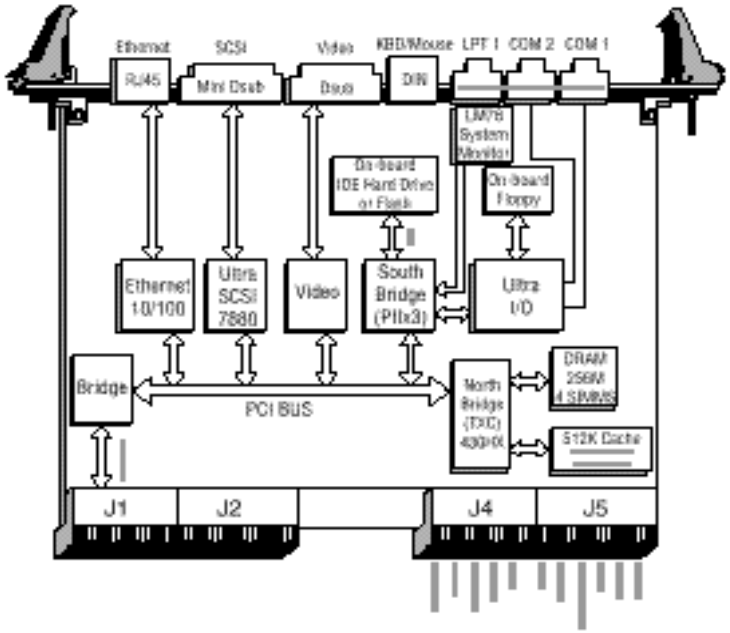
Implementation of HDR LOS Prototype Modem

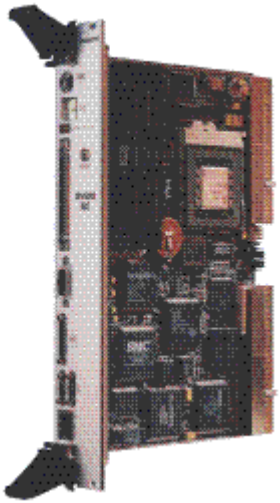
- **Contractor:** Nova Engineering, Cincinnati, OH
- 6U cPCI Modules
  - Pentium Control Processor (COTS)
    - CPV5000 with Ethernet Interface
  - Master Demodulator (HSP Module)
  - Slave Demodulator (HSP Module)
  - Modulator (HSP Module)
  - Packet Processor (HSP Module)
  - IF Assembly Module
- Chassis (COTS)
  - CPV2108 from Motorola

- Three to be delivered in Mar 99 with OFDM waveform

Control Module

- **Specifications: CPV5000 by Motorola (COTS)**
  - **6U Single-Board Computer**
  - **233 MHz Pentium MMX Processor**
  - **Up to 256 MB DRAM**
  - **512 KB Cache**
  - **10/100 Base-T Ethernet**
  - **SVGA Video**
  - **2 USB Ports**
  - **2 COM Ports**
  - **EIDE Interface**
  - **cPCI 2.1 Compliant**
  - **Watch Dog Monitor**



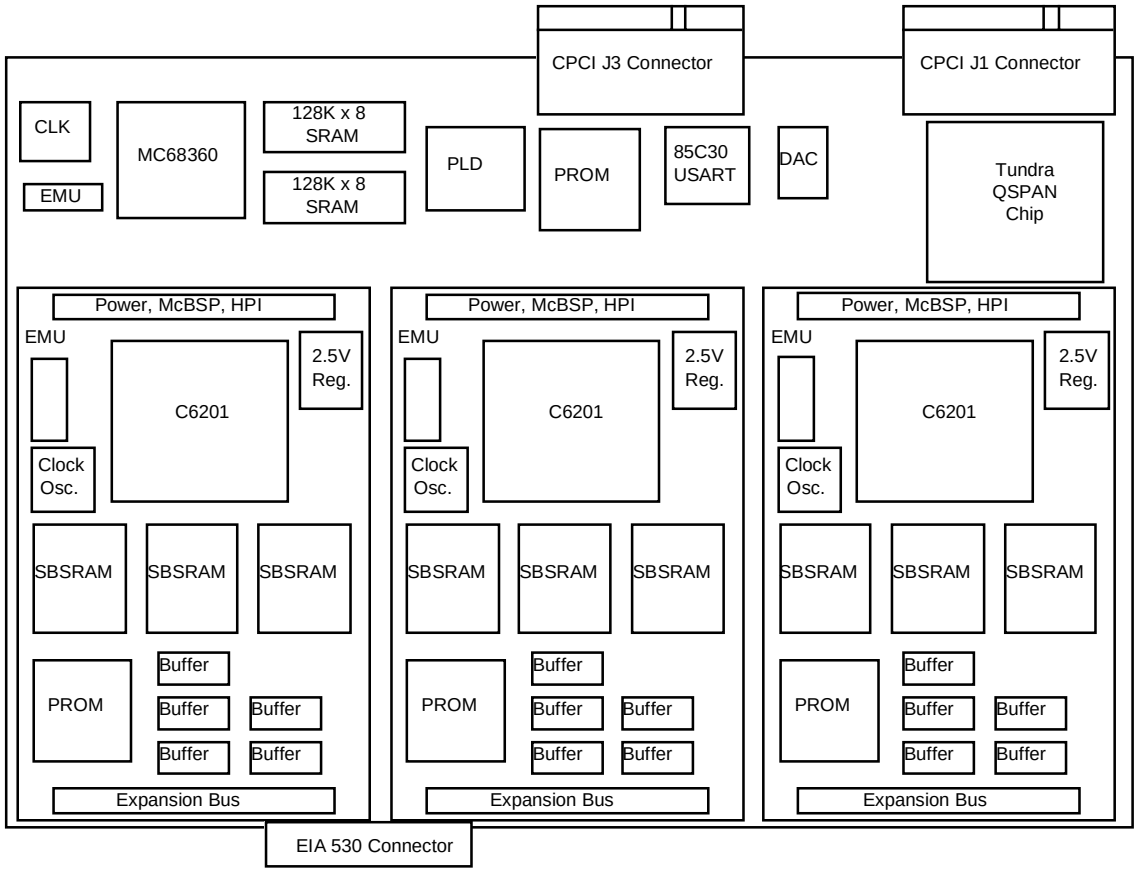


CPV5000 Block Diagram

High Speed Processor (HSP) Module Summary

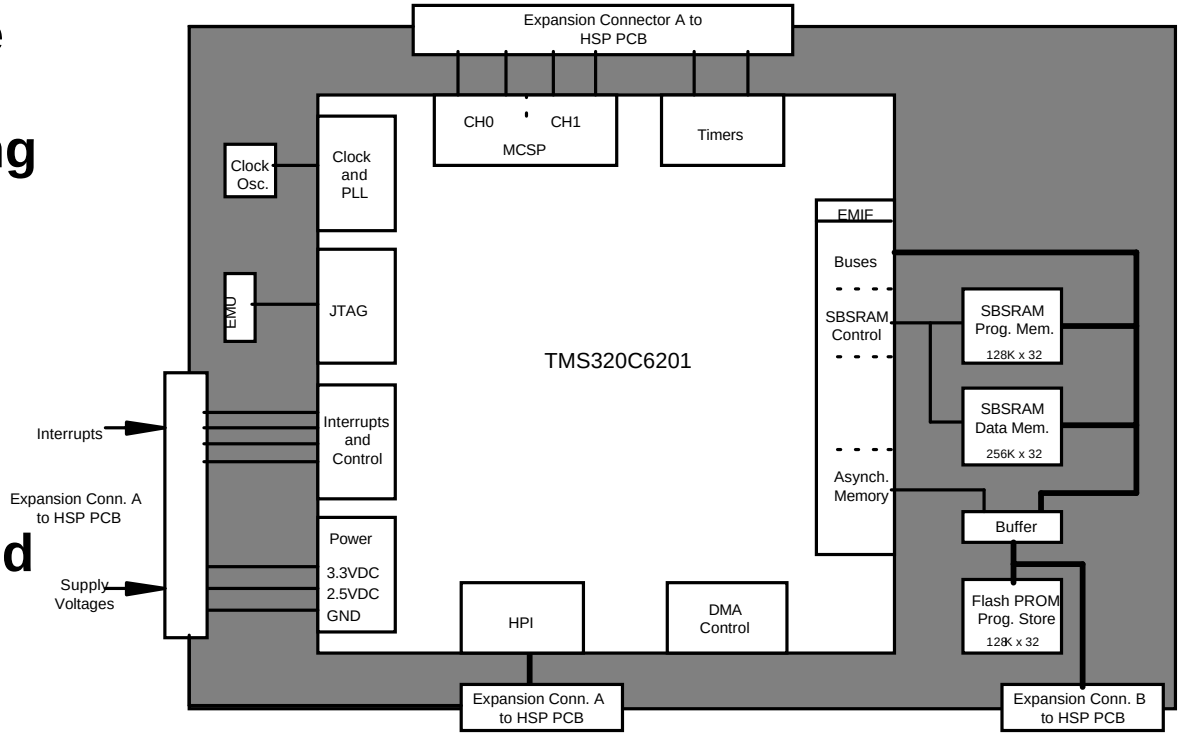
- Contractor: Nova Engineering
- HSP implemented as a 6U cPCI bus board with three DSP daughter cards (DSPU's).
- Features:
  - Sites for three DSPUs at 1600 MIP's each.
  - Integrated PCI bus interface: Tundra QSPAN chip
  - Local control processor: MC68360
  - J1 system 32-bit bus connection, J3 private inter-card communications using 'C6201 serial Ports
  - EIA 530 Serial Interface controlled by MC68360
- cPCI Physical Size: 233 mm x 160 mm (6U)
- DSPU Physical Size: 2.5 in. x 4.0 in.
- Nova will offer this assembly for sale commercially.

HSP 6U cPCI Module

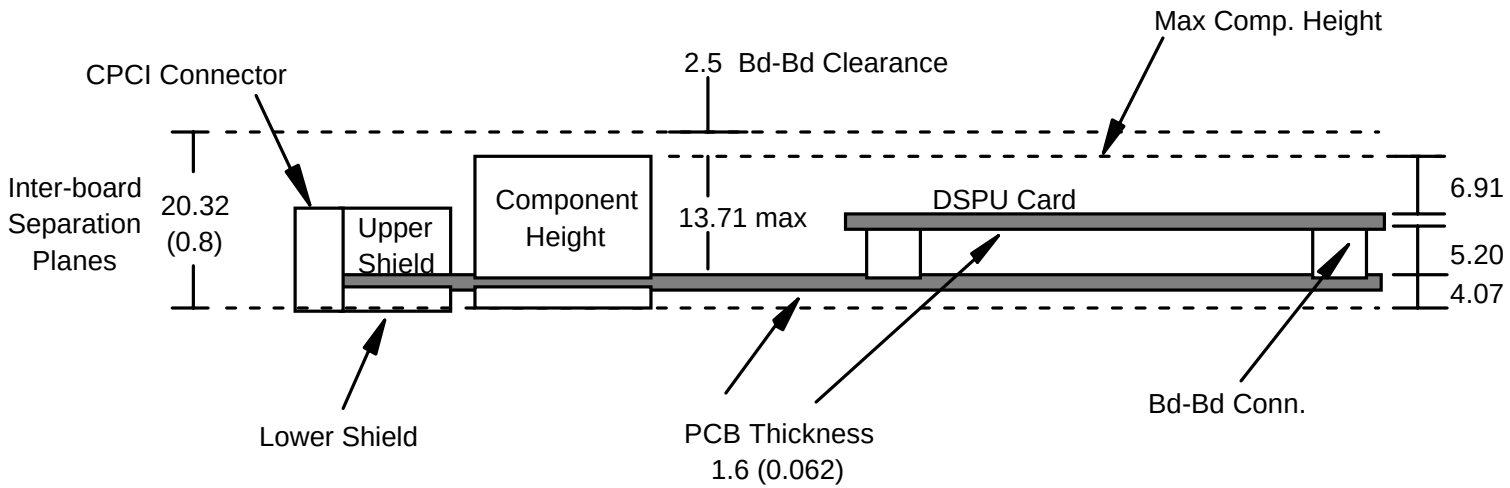


DSPU Card Summary

- Contractor: Nova Engineering
- Features:
  - TMS320C6201 DSP, 128K x 32 code RAM, 256K x 32 data RAM.
  - Buffered expansion connection to main HSP board.
  - Allows for more PCB area effectively creating two planes for circuitry.
  - Separate DSPU card simplifies debugging task and eases manufacturing and testing.



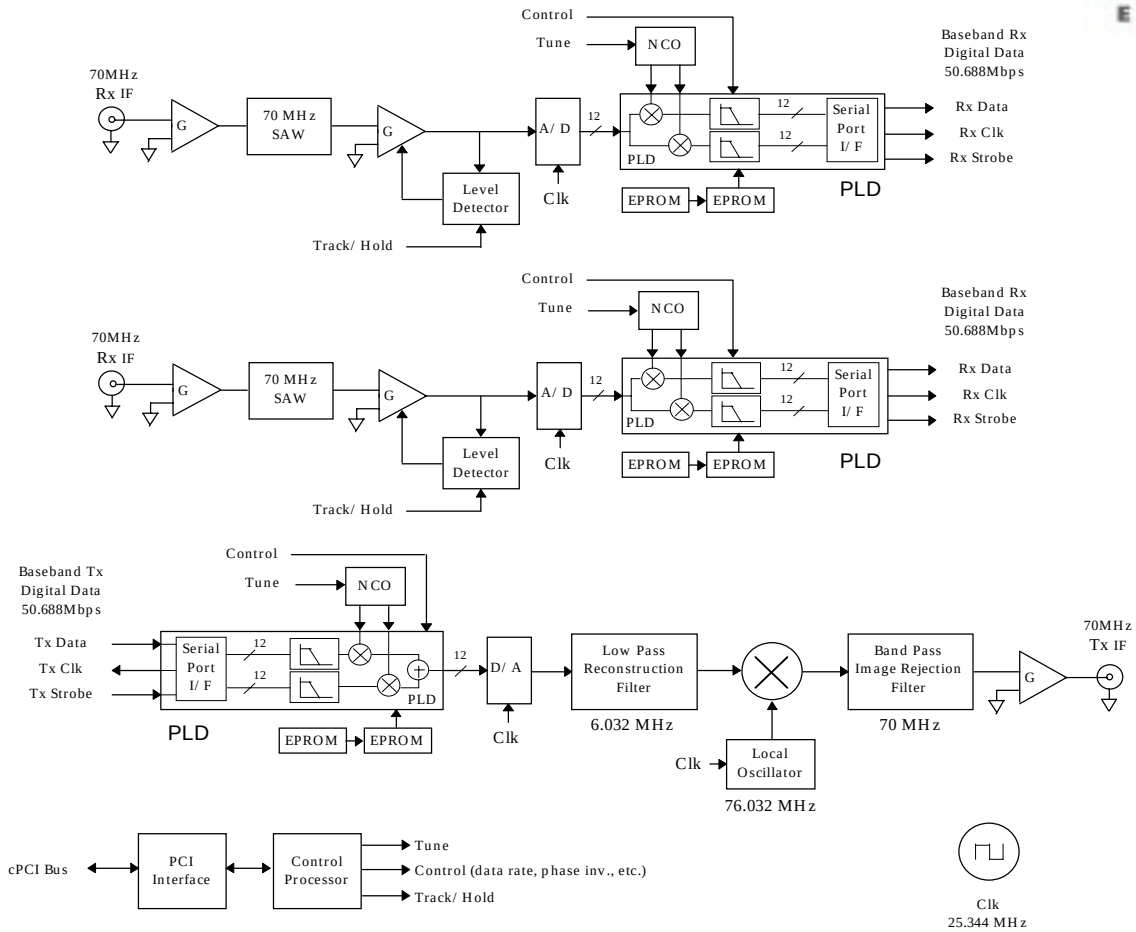
HSP 6U cPCI Module Mechanical Diagram



IF Module Summary

- **Dual Diversity Receiver - provides improved performance in presence of multipath**
  - Each IF Assembly has 2 complete Rx channels and 1 Tx channel
- **Supports 9 different Channel Bandwidths**
  - 2.0 MHz, 1.8 MHz, 1.2 MHz, 1.0 MHz, 600 kHz, 225 kHz, 200 kHz, 50 kHz, 25 kHz
- **Bandpass Sampling**
  - 12-bits @ 25Msps
  - filtering, decimation, and interpolation all implemented in reprogrammable PLDs (Altera 10K100) using VHDL
- **Digital Frequency Conversion - eliminates problems associated with analog conversion**
  - I/Q phase imbalance, DC offset, component tolerance, temperature variation, aging, calibration
- **Standard Interfaces**
  - Integrated cPCI Interface, 70MHz IF
- **Additional Features**
  - Test modes include Rx-Tx loopback, two tone Tx output
  - Fast attack AGC with track and hold modes
  - Digitally monitored RSSI

IF Module
Block Diagram



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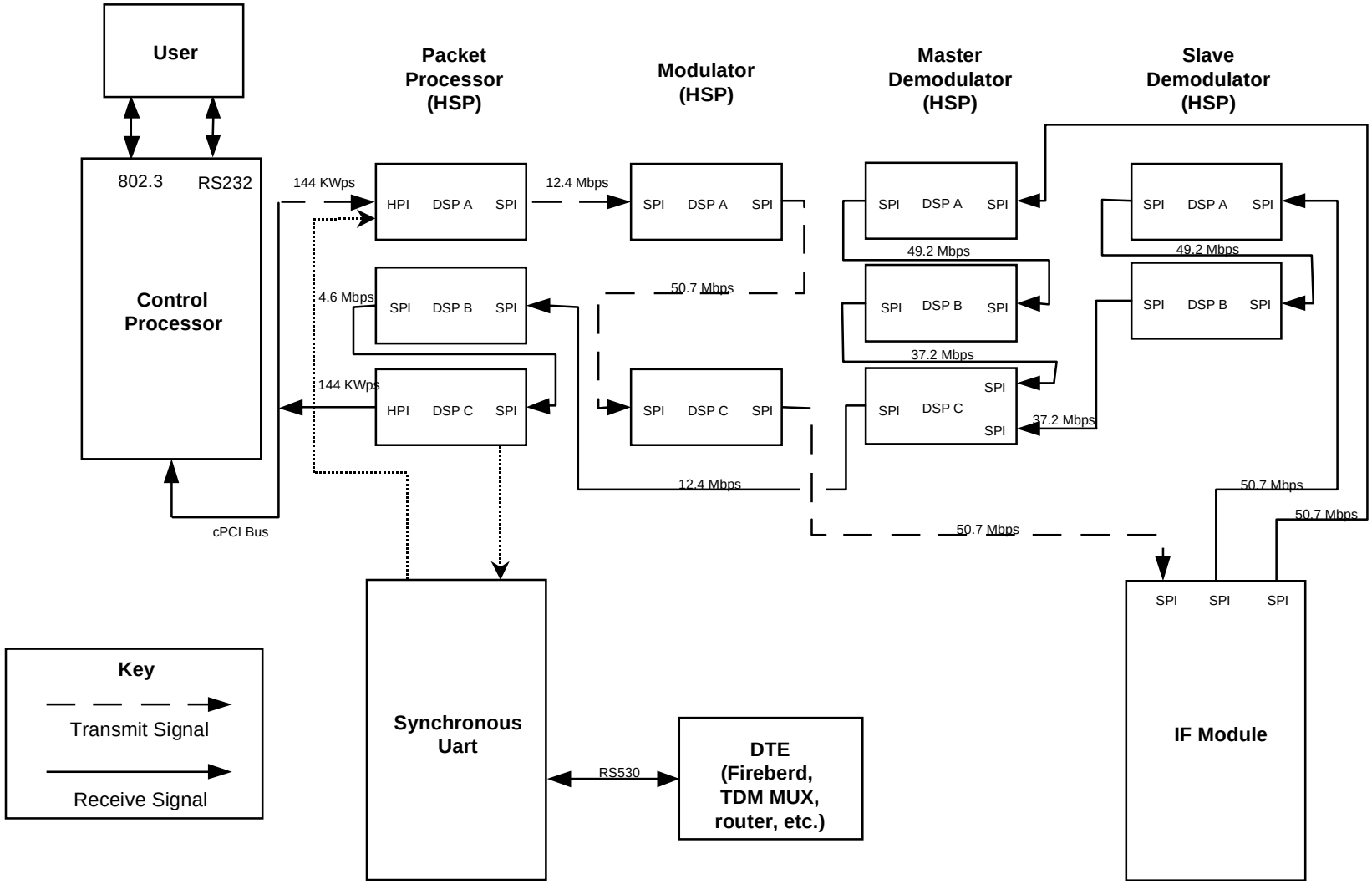
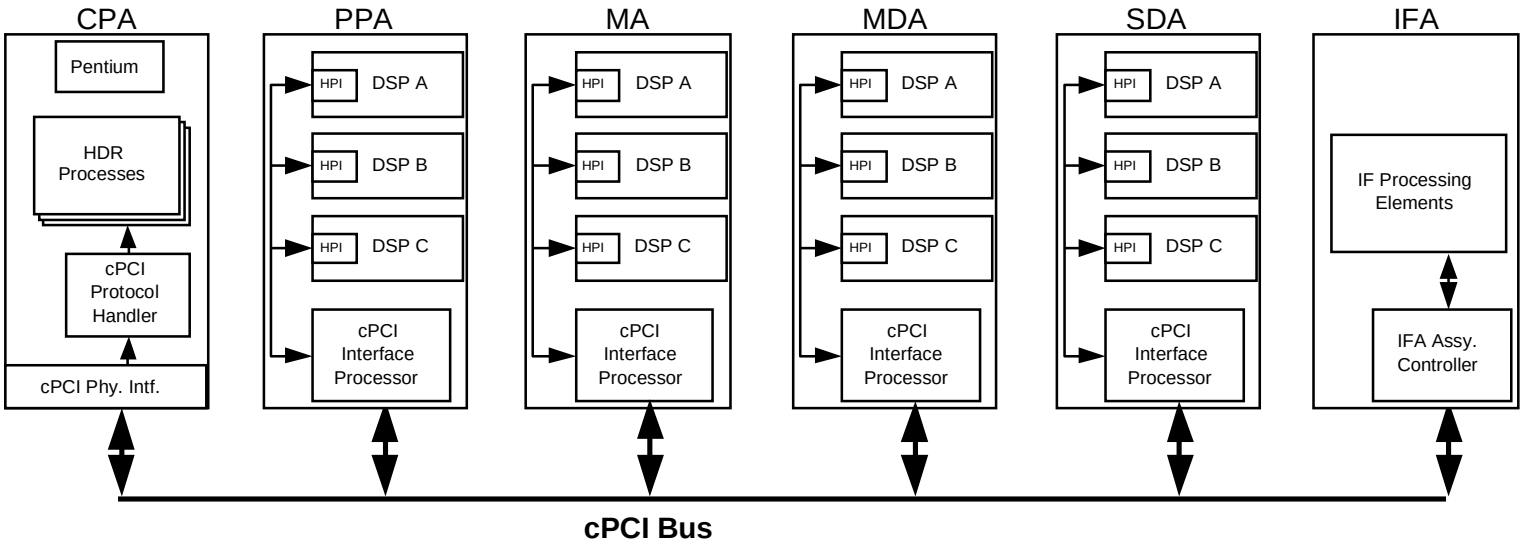
Modem
Software Development

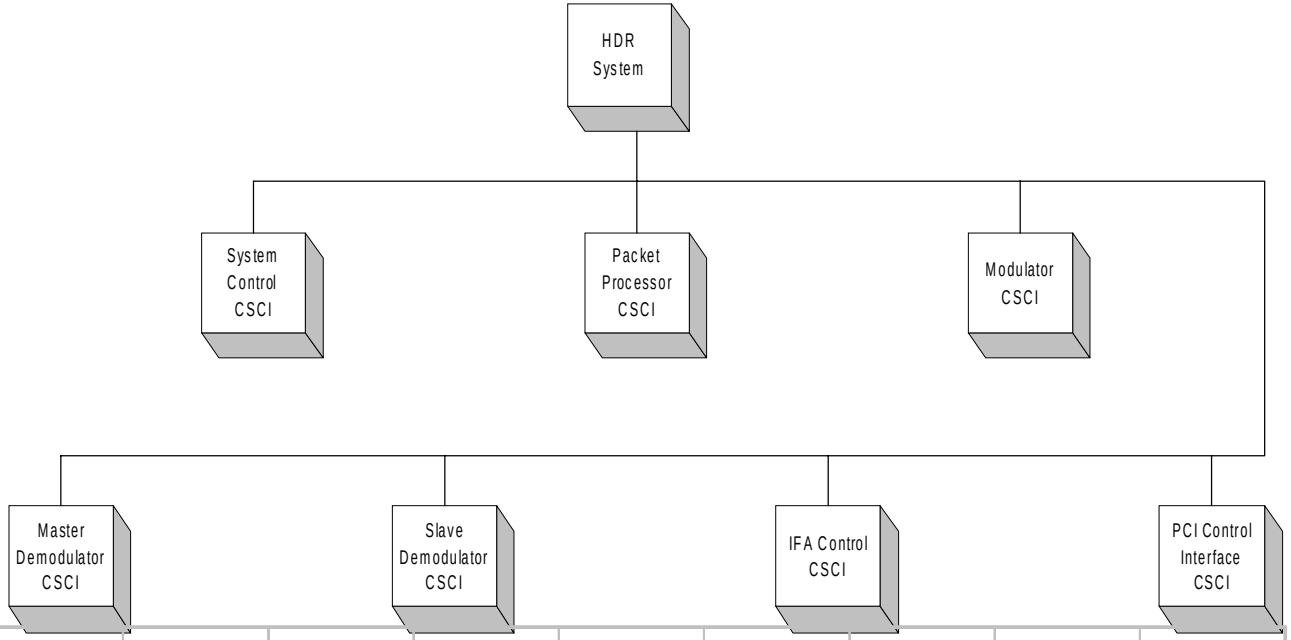
Modem System Signal Flow



Modem System Control Flow

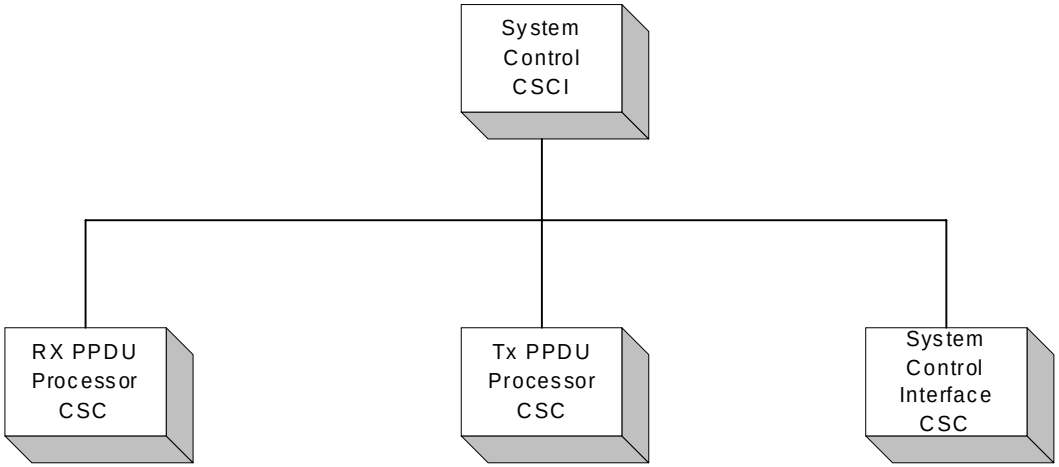


CSCI Level Functional Allocation



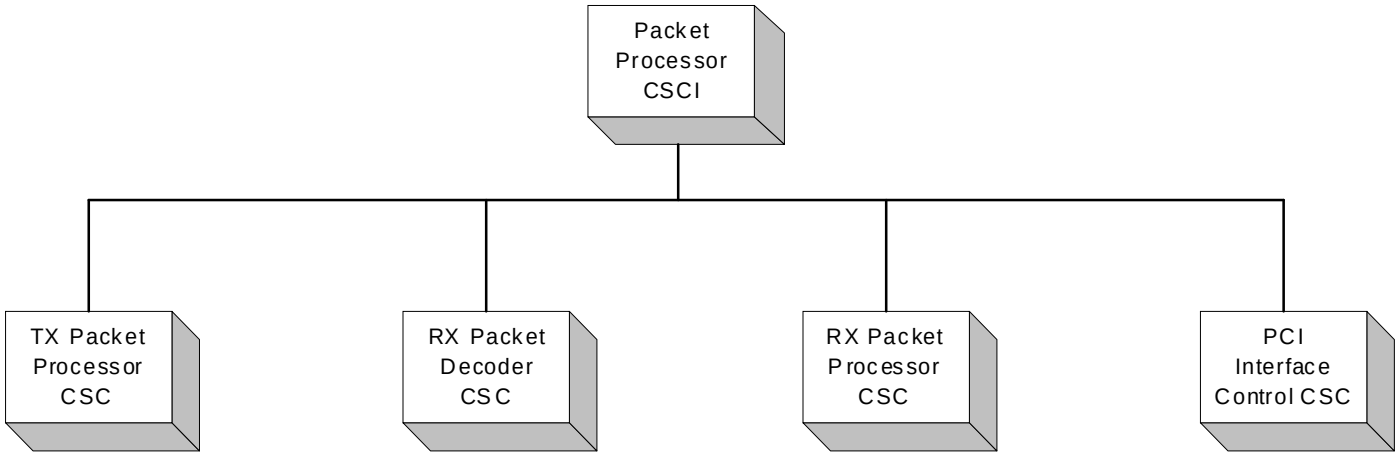
CSCI	System Control	Packet Processor	Modulator	Master Demod	Slave Demod	IFA Control	cPCI Control Interface
Phy. Resource	Control Processor Assy.	HSPA	HSPA	HSPA	HSPA	IFA Assy.	All except Control Processor & Ext Intf Assy.
Function	Ext. Data I/O Mgmt.	Tx Packet Proc., Ext. Data I/O Mgmt	Tx Modulation	Tx Freq. & Timing Recovery	Tx Freq. & Timing Recovery	IFA Assy. Controller	cPCI/Host Control
Function	Sys. Cntl User Interface	Rx Packet Proc.	Tx Signal Preproc.	Rx Signal Demod	Rx Signal Demod		

System Control CSCI Decomposition



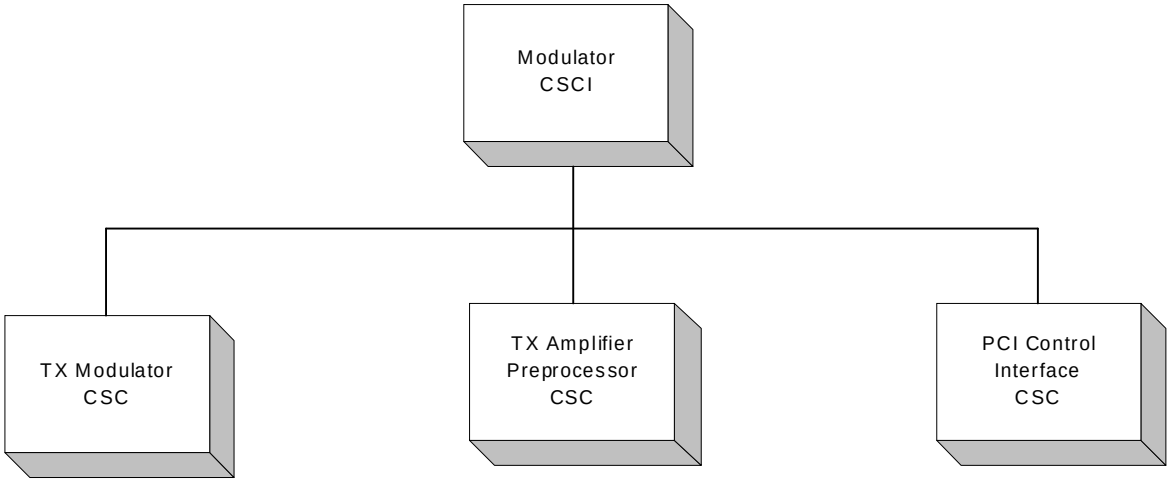
CSC	RxPPDU	TxPPDU	System Control UI
Phy. Resource	Control Processor Assy. CPU	Control Processor Assy. CPU	Control Processor Assy. CPU
Function	Packetize / DePacketize	Packetize / DePacketize	Sys. Cntl User Interface

Packet Processor CSCI Decomposition



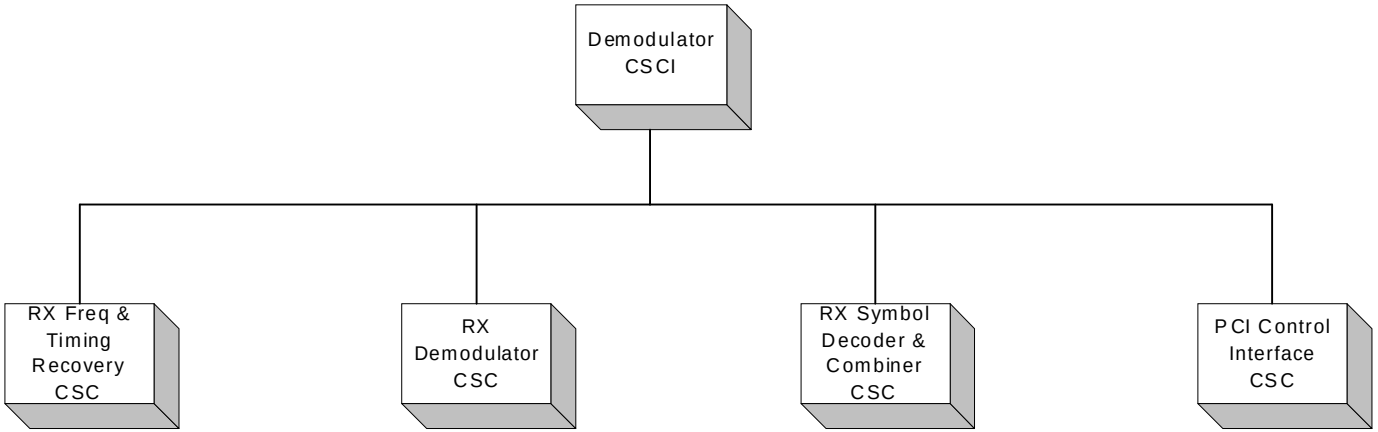
CSC	Tx Packet Processor	Rx Packet Processor	Rx Packet Decode	cPCI Control Interface
Phy. Resource	DSP A	DSP C	DSP B	cPCI Bus Interface Proc
Function	Transmit Packet Processing	Ext. Data I/O Mgmt.	Tx Packet Proc.	cPCI/HSPA Interface Control

Modulator CSCI Decomposition



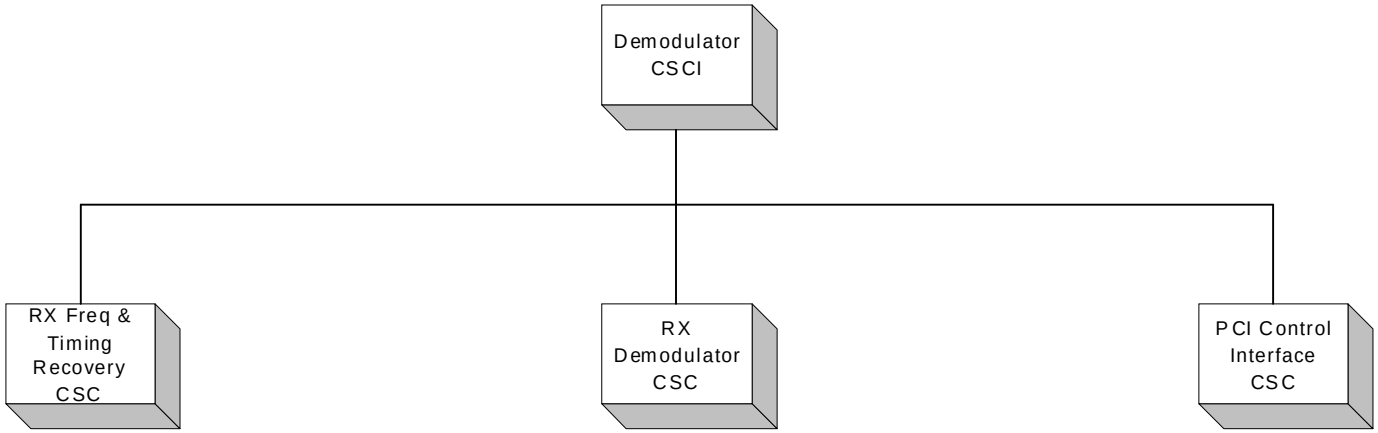
CSC	Tx Modulator	Rx Packet Processor	cPCI Control Interface
Phy. Resource	DSP A	DSP C	cPCI Bus Interface Proc
Function	Transmit data modulation	Transmit signal preproc	cPCI/HSPA Interface Control

Master Demodulator CSCI Decomposition



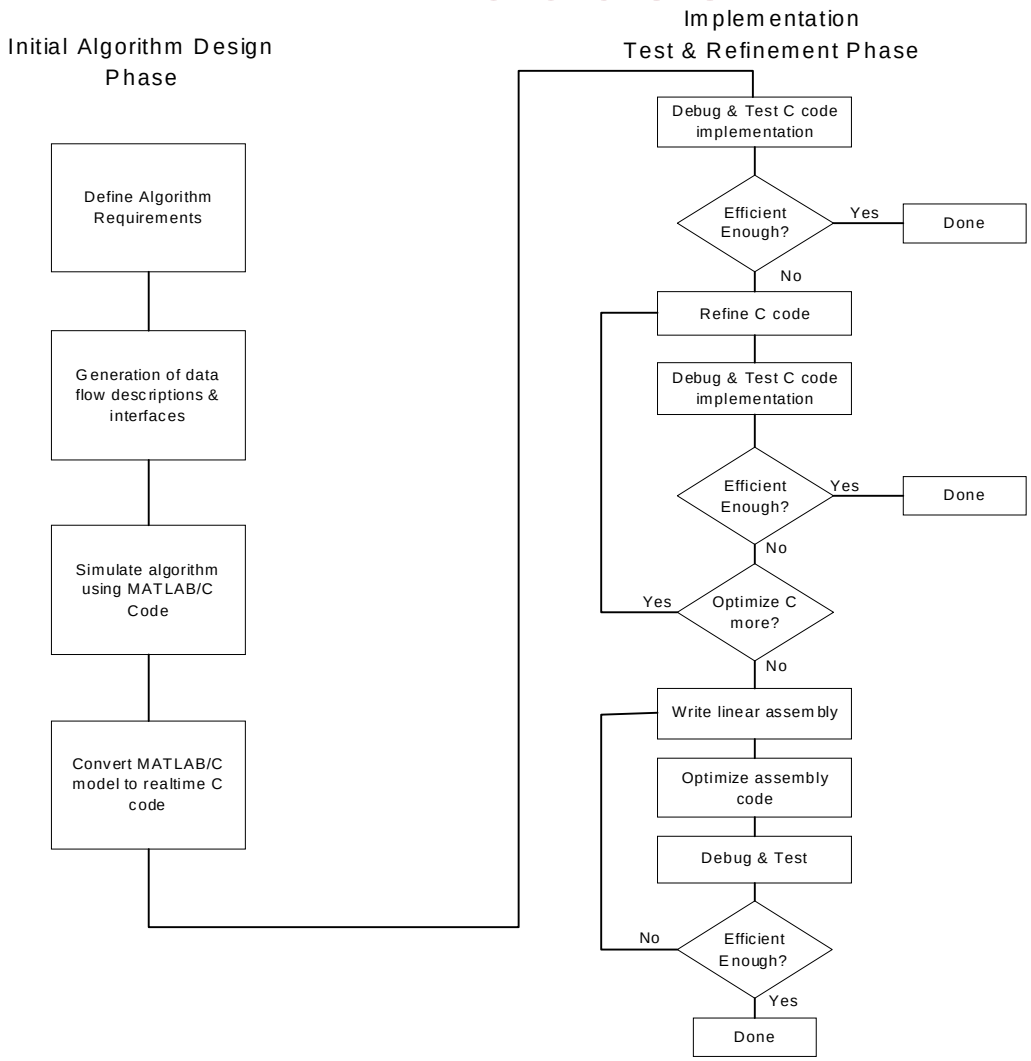
CSC	Rx Freq. & Timing Recovery	Rx Demod.	Rx Sym. Decoder & Combiner	cPCI Control Interface
Phy. Resource	DSP A	DSP B	DSP C	cPCI Bus Interface Proc
Function	Receive signal frequency & timing recovery	Receive signal demod.	OFDM symbol decoder & combiner	cPCI/HSPA Interface Control

Slave Demodulator CSCI Decomposition



CSC	Rx Freq. & Timing Recovery	Rx Demod.	cPCI Control Interface
Phy. Resource	DSP A	DSP B	cPCI Bus Interface Proc
Function	Receive signal frequency & timing recovery	Receive signal demod.	cPCI/HSPA Interface Control

DSP Algorithm Development Process



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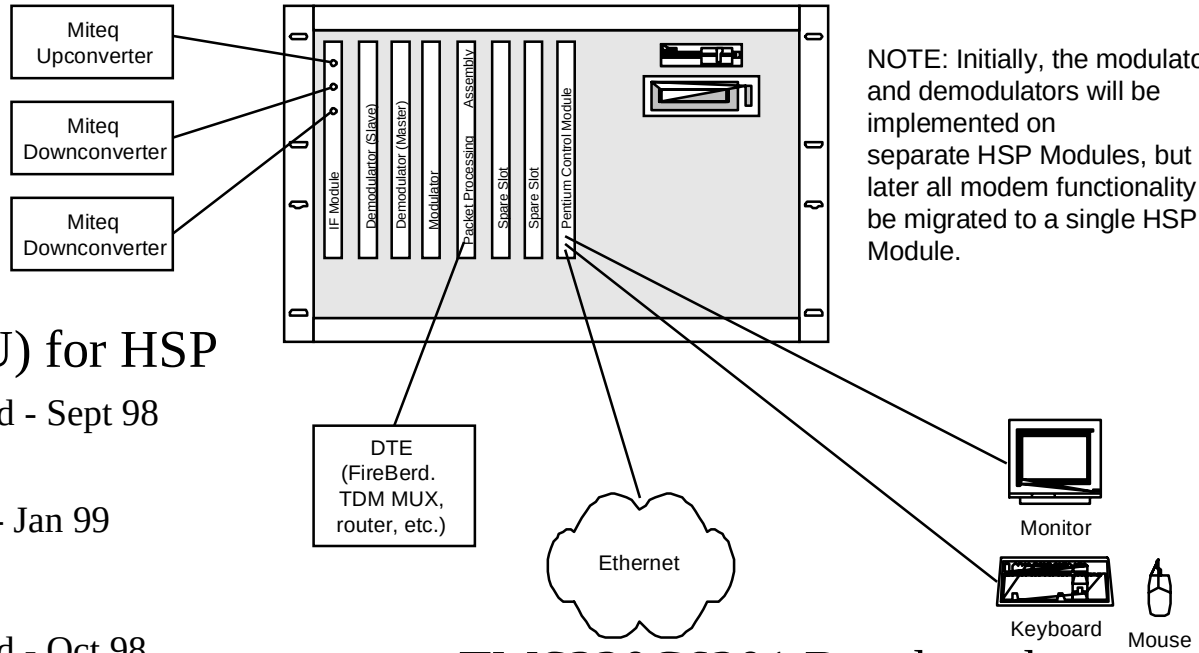
Software Development Tools

- DSP Processor Software
  - TMS320C6201(TI DSP)
    - TI C Compiler, Assembler, Linker
    - TI Source Debugger, Code Composer
    - White Mountain 510 Emulator
  - MC68360 (Motorola Communications Controller)
    - MicroTek C Compiler, Assembler, Linker
    - MicroTek Source Debugger
- PLD Software
  - Altera 10K100A-1
    - Altera MaxPlus II (VHDL, Design, Simulation, Place & Route)
- Other
  - Windows NT Software
    - Microsoft Developer Studio
    - Microsoft Visual C++
  - Configuration Control Software
    - Microsoft Visual SourceSafe
    - Premia Codewrite 5.0
  - Simulation Tools
    - MathWorks MATLAB
    - Metroworks CodeWarrior

HDR LOS Modem Status

(as of Oct 98)



NOTE: Initially, the modulator and demodulators will be implemented on separate HSP Modules, but later all modem functionality will be migrated to a single HSP Module.

- Daughter Card (DSPU) for HSP
  - hardware 100% completed - Sept 98
  - software drivers - Oct 98
  - OFDM modem software - Jan 99
- HSP Module
  - hardware 100% completed - Oct 98
  - software drivers, I/O - Nov 98
  - CPCI interface software - Nov 98
- IF Module
  - hardware 100% completed - Aug 98
  - Start performance testing - Oct 98
  - Complete testing - Dec 98
- TMS320C6201 Benchmarks
  - 100% complete
  - FFT processing with Full Speed Serial I/O
- OFDM Waveform
  - 95% complete - simulation and documentation for 600 KHz modes
  - Additional modem features - Feb 99
  - Testing - March 99